L Number	Hits	Search Text	DB	Time stamp
1	524	voltage adj variable adj capacitor	USPAT; US-PGPUB	2004/06/24 14:30
2	491	(voltage adj variable adj capacitor) and @ad<20020814	USPAT; US-PGPUB	2004/06/24 13:51
3	117	((voltage adj variable adj capacitor) and @ad<20020814) and substrate and well	USPAT; US-PGPUB	2004/06/24 13:42
4	40	(((voltage adj variable adj capacitor) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide))	USPAT; US-PGPUB	2004/06/24 13:42
5	2302	varactor adj diode	USPAT; US-PGPUB	2004/06/24 14:28
6	2168	(varactor adj diode) and @ad<20020814	USPAT; US-PGPUB	2004/06/24 13:42
7	374	((varactor adj diode) and @ad<20020814) and substrate and well	USPAT; US-PGPUB	2004/06/24 14:28
8	135	(((varactor adj diode) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide))	USPAT; US-PGPUB	2004/06/24 13:43
9	128	((((varactor adj diode) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide))) not ((((voltage adj variable adj capacitor) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide)))	USPAT; US-PGPUB	2004/06/24 13:43
10	4728	varactor	USPAT; US-PGPUB	2004/06/24 14:29
11	366	varactor and @ad<20020814 and substrate and (isolation or (field adj oxide))	USPAT; US-PGPUB	2004/06/24 13:51
12	325	(varactor and @ad<20020814 and substrate and (isolation or (field adj oxide))) and well	USPAT; US-PGPUB	2004/06/24 13:51
13	198	((varactor and @ad<20020814 and substrate and (isolation or (field adj oxide))) and well) not (((((varactor adj diode) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide))) not ((((voltage adj variable adj capacitor) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide))))	USPAT; US-PGPUB	2004/06/24 13:52
14	175	(((varactor and @ad<20020814 and substrate and (isolation or (field adj oxide))) and well) not (((((varactor adj diode) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide))) not ((((voltage adj variable adj capacitor) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide))))) not ((((voltage adj variable adj capacitor) and @ad<20020814) and substrate and well) and (isolation or (field adj oxide)))	USPAT; US-PGPUB	2004/06/24 13:52
15	2201	varactor adj diode	EPO; JPO; DERWENT; IBM_TDB	2004/06/24 14:28
16	1	(varactor adj diode) and substrate and well and (isolation or (field adj oxide))	EPO; JPO; DERWENT; IBM_TDB	2004/06/24 14:29
17	3413	varactor	EPO; JPO; DERWENT; IBM_TDB	2004/06/24 14:29
18	2	varactor and substrate and well and (isolation or (field adj oxide))	EPO; JPO; DERWENT; IBM_TDB	2004/06/24 14:30
19	160	voltage adj variable adj capacitor	EPO; JPO; DERWENT; IBM_TDB	2004/06/24 14:30
20	0	(voltage adj variable adj capacitor) and substrate and well and (isolation or (field adj oxide))	EPO; JPO; DERWENT; IBM_TDB	2004/06/24 14:30

US-PAT-NO: 5965912

DOCUMENT-IDENTIFIER: US 5965912 A

TITLE: Variable capacitor and method for fabricating the same

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Abstract Text - ABTX (1):

A **voltage variable capacitor** (10) fabricated on a semiconductor substrate (11) includes a gate structure (62) and a **well** (22) under the gate structure (62). A heavily doped buried layer (15) and a heavily doped contact region (31) in the semiconductor substrate (11) form a low resistance conduction path from the **well** (22) to a surface (17) of the semiconductor substrate (11). A multi-finger layout is used to construct the **voltage variable capacitor** (10). In operation, when a voltage applied across the **voltage variable capacitor** (10) changes, the width of depletion region in the **well** (22) changes, and the capacitance of the **voltage variable capacitor** (10) varies accordingly.

Brief Summary Text - BSTX (5):

Accordingly, it would be advantageous to have a **voltage variable capacitor** and a method for fabricating the capacitor. It is desirable for the capacitor to have a high quality factor and a low leakage. It is also desirable for the capacitor to have a large capacitance variation range over a small voltage range. It is further desirable for the capacitor to be fabricated with other integrated circuit devices in a monolithic semiconductor chip. It would be of further advantage for the method to be compatible with

existing semiconductor
integrated circuit fabrication processes.

Detailed Description Text - DETX (2):
Generally, the present invention provides a **voltage variable capacitor** and a
method for fabricating the **voltage variable capacitor**. The **voltage variable**
capacitor is Metal Oxide on Semiconductor (MOS) capacitor fabricated on a
semiconductor substrate. A gate structure serves as a top plate of the
capacitor, and a **well** under the gate structure serves as a bottom plate of the
capacitor. When the gate structure includes a polycrystalline silicon layer,
the **voltage variable capacitor** is referred to as a singly poly capacitor. A
heavily doped buried layer and a heavily doped contact region of the same
conductivity type as the **well** form a low resistance conduction path from the
well to the surface of the semiconductor substrate. To further reduce the
series resistance and increase the quality factor (Q) of the **voltage variable**
capacitor, a multi-finger layout is preferably used to construct the **voltage**
variable capacitor. In operation, when a voltage applied across the top and
bottom plates changes, the width of depletion region in the **well** changes, and
the capacitance of the **voltage variable capacitor** varies accordingly.
Preferably, the **voltage variable capacitor** is fabricated with other
semiconductor devices, e.g., field effect transistors, bipolar transistors,
resistors, inductors, or the like, on an integrated circuit chip. Therefore,
the **voltage variable capacitor** is also referred to as a monolithic **voltage**
variable capacitor.

Detailed Description Text - DETX (3):

A **voltage variable capacitor** 10 in accordance with the present invention is schematically shown in FIGS. 1 and 2. More particularly FIG. 1 is a schematic top view of **voltage variable capacitor** 10, and FIG. 2 is a schematic cross-sectional view of **voltage variable capacitor** 10 along a section-line 2--2. It should be noted that the figures are not drawn to scale and that the same reference numerals are used in the figures to represent elements of similar structures and functions.

Detailed Description Text - DETX (4):

Voltage variable capacitor 10 is fabricated in a body 11 of semiconductor material. Body 11 of semiconductor material includes a semiconductor substrate 12. By way of example, semiconductor substrate 12 is a P conductivity type silicon substrate having a dopant concentration between approximately 1.times.10.sup.15 atoms per cubic centimeter (atoms/cm.sup.3) and approximately 1.times.10.sup.17 atoms/cm.sup.3. Ions of N conductivity type such as, for example, phosphorus ions or arsenic ions, are implanted into semiconductor substrate 12 adjacent its front surface 14. The implanted ions form a doped layer 15 in semiconductor substrate 12 adjacent to front surface 14. Doped layer 15 has a dopant concentration between, for example, approximately 1.times.10.sup.19 atoms/cm.sup.3 and approximately 5.times.10.sup.22 atoms/cm.sup.3. Body 11 of semiconductor material also includes a layer 16 of semiconductor material epitaxially grown on front surface 14 of semiconductor substrate 12. A major surface 17 of epitaxial layer 16 is also referred to as a major surface of body 11 of semiconductor material. Epitaxial layer 16 buries doped layer 15. Thus, doped layer 15 is also referred to as a buried

layer. The thickness of epitaxial layer 16 is substantially equal to the depth of buried layer 15. By way of example, the depth of buried layer 15 ranges between approximately 500 nanometers (nm) and approximately 3,000 nm. It should be noted that body 11 of semiconductor material comprised of semiconductor substrate 12, buried layer 15, and epitaxial layer 16 can also be referred to as a semiconductor substrate or simply a substrate.

Detailed Description Text - DETX (5):

Field oxide regions 18 are formed over the portions of epitaxial layer 16 in a Local Oxidation of Silicon (LOCOS) process. **Field oxide** regions 18 provide **isolation** structures between **voltage variable capacitor** 10 and other devices (not shown) fabricated on substrate 11. An ion implantation is optionally performed before forming **field oxide** regions 18 to form heavily doped regions (not shown) under **field oxide** regions 18. The heavily doped regions (not shown) prevent inadvertent turning on of parasitic field effect transistors formed under **field oxide** regions 18. It should be understood that the **isolation** structures on substrate 11 can be formed using other processes such as, for example, poly-buffered LOCOS, poly-encapsulated LOCOS, trenching, etc.

Detailed Description Text - DETX (6):

Ions of N conductivity type such as, for example, phosphorus ions or arsenic ions are selectively implanted into epitaxial layer 16 to form N-conductivity type **wells** 22, 24, 26, and 28. **Wells** 22, 24, 26, and 28 extend from major surface 17 into epitaxial layer 16 and reach buried layer 15. The dopant concentration of **wells** 22, 24, 26, and 28 is between, for example,